S/N 08/984,562 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jeffrey S. Mailloux et al.	Examiner: Hong Kim	
Serial No.:	08/984,562	Group Art Unit: 2751	
Filed:	December 3, 1997	Docket: 303.623US3	
Title:	MEMORY DEVICE FOR BURST OR PIPELINED OPERATION WITH MODE SELECTION CIRCUITRY		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

#19 Amdt 5-7-01 OC

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on February 1, 2001. Please amend the above-identified patent application as follows.

IN THE SPECIFICATION

Please substitute the following paragraphs of the Specification with the paragraphs in the appendix entitled Clean Version of Specification Paragraphs. Following are marked-up paragraphs of the Specification.

Paragraph beginning on page 29, line 8 is amended as follows:

If mode select is active high (e.g., logic "1"), pipelined EDO mode is selected for operation of memory 100. Control logic 121 in response to receiving mode select pipelined information, provides newburst signal 110 to [MUX 123] buffer 122 to select external input XA0-XAn. In this manner an external address via ADDR signal 115 may be sent through buffer 122 to decoder 104 for each /CAS signal 114 cycle for pipelined EDO mode. In other words, a new external column address for memory array 111 may be provided for each access to memory 100. Thus, while memory 100 is in pipelined EDO mode, newburst signal 110 instructs buffer 122 to select address inout only from ADDR signal 115.